Patent
Attorney's Docket No. F0255

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

UTILITY PATENT
APPLICATION TRANSMITTAL LETTER

Box PATENT APPLICATION
Commissioner for Patents
Washington, D.C. 20231

Sir:

Enclosed for filing is the utility patent application of Feng-Jong Edward YANG and Bahadir ERIMLI for METHOD AND APPARATUS FOR ACCESSING EXTERNAL MEMORIES.

Also enclosed are:

[X] 5 sheet(s) of [ ] formal [X] informal drawing(s);

[ ] claim for foreign priority under 35 U.S.C. §§ 119 and/or 365 [ ] hereby made to _____ filed in _____ on _____;

[ ] in the declaration;

[ ] a certified copy of the priority document;

[ ] a General Authorization for Petitions for Extensions of Time and Payment of Fees;

[ ] _____ statement(s) claiming small entity status;

[X] an Assignment document and Assignment Recordation Cover Sheet;

[X] an Information Disclosure Statement, PTO-1449, and 1 document; and

[ ] Other:_____;

[X] An [X] executed [ ] unexecuted Declaration and Power of Attorney of the inventor(s).

[ ] Please amend the specification by inserting before the first line the sentence –This application claims priority under 35 U.S.C. §§ 119 and/or 365 to _____ filed in _____ on _____; the entire content of which is hereby incorporated by reference.--

[ ] A bibliographic data entry sheet is enclosed.

[X] The filing fee has been calculated as follows [ ] and in accordance with the enclosed preliminary amendment:

CLAIMS					
	NO. OF CLAIMS		**EXTRA CLAIMS**	**RATE**	**FEE**
Basic Application Fee					$690.00 (101)
Total Claims	20	MINUS 20 =	0	x $18.00 (103)	0
Independent Claims	3	MINUS 3 =	0	x $78.00 (102)	0
If multiple dependent claims are presented, add $260.00 (104)					
Total Application Fee					$690.00
If verified Statement claiming small entity status is enclosed, subtract 50% of Total Application Fee					
Add Assignment Recording Fee if Assignment document is enclosed					$40.00
TOTAL APPLICATION FEE DUE					$730.00

[ ] This application is being filed without a filing fee. Issuance of a Notice to File Missing Parts of Application is respectfully requested.

[X] A check in the amount of $ 730.00 is enclosed for the fee due.

[ ] Charge $_____ to Deposit Account No. 50-1070 for the fee due.

[X] The Commissioner is hereby authorized to charge any appropriate fees under 37 C.F.R. §§ 1.16, 1.17, and 1.21 that may be required by this paper, and to credit any overpayment, to Deposit Account No. 50-1070. This paper is submitted in duplicate.

Respectfully submitted,

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F0255

METHOD AND APPARATUS FOR ACCESSING EXTERNAL MEMORIES

TECHNICAL FIELD

The present invention relates generally to network communications and, more particularly, to accessing external memories via a network switch.

BACKGROUND ART

In computer networks, a number of network stations are typically interconnected via a communications medium. For example, Ethernet 802.3 is a commonly used local area network (LAN) scheme in which multiple stations are connected to a shared serial data path. These stations often communicate with a switch located between the data path and the stations connected to that path. The switch typically controls the communication of data and includes logic for receiving and forwarding data frames to their appropriate destinations.

When all of the stations connected to the network are simultaneously operating, data traffic on the shared serial path can be heavy with little time between data frames. Accordingly, some switches transfer the data frames to an external memory for storage to reduce on-chip memory requirements. The data frames must then be transferred back to the switch before transmitting the frames to their respective destinations. With increased network throughput requirements, such a processing arrangement often results in an unacceptable delay in forwarding the data frames.

One conventional way of reducing the time for processing data frames is to increase the width of the external memory bus. For example, as the number of ports supported by the switch increases, the data width of the external memory bus typically increases so that the data transfer rate is able to keep up with both the inbound and outbound packet rates.

As the width of the external memory bus increases, however, the bus efficiency decreases due to transfers involving the last few bytes of a data frame. For example, assume that the external memory bus is 16 bytes wide and the switch receives a data

frame 65 bytes in length. In this case, five separate transfers are required to store all of the data to the external memory. On the last transfer, however, only one byte of meaningful data is transferred with the other 15 bytes being wasted. Accordingly, the bus efficiency for such a frame is 65/(5 X 16) or 81.25%. If all the ports receive similar packets, the switch resources will be used up transferring meaningless data and the data throughput of the switch will be significantly reduced.

Another drawback with increasing the width of the external memory bus involves memory management overhead. Each data frame stored to external memory typically includes a buffer header used for memory management. The buffer header may include information such as the address of the next buffer storing a portion of the data frame, the last buffer bit, etc. This buffer header information is usually a few bytes in length. When updating the buffer header or when accessing the header information for retrieving the stored data frame, only the few header bytes are transferred over the external memory bus with the remaining bytes being zero filled or filled with other meaningless data. This further decreases the bus efficiency and wastes valuable bandwidth.

DISCLOSURE OF THE INVENTION

There exists a need for a system and a method for increasing the efficiency associated with transferring data to and from an external memory while maintaining high data throughput.

These and other needs are met by the present invention, where a multiport switch includes an external memory interface that simultaneously transfers data frame information to two external memories to increase the bus efficiency and meet network bandwidth requirements.

According to one aspect of the present invention, a network switch controls communication of data frames between stations. The switch includes a plurality of receive devices corresponding to ports on the network switch. The receive devices are configured to receive data frames from the stations. The switch also includes an external memory interface configured to receive data from the plurality of receive devices, transfer a portion of the data received from a first one of the receive devices to a first memory, and transfer a portion of the data received from a second one of the receive devices to a second memory.

Another aspect of the present invention provides a method for storing data frame information received by a network switch that controls the communication of data frames. The method includes receiving a plurality of data frames and temporarily storing the received data frames. The method also includes simultaneously transferring data frame information to at least a first memory and a second memory.

Other advantages and features of the present invention will become readily apparent to those skilled in this art from the following detailed description. The embodiments shown and described provide illustration of the best mode contemplated for carrying out the invention. The invention is capable of modifications in various obvious respects, all without departing from the invention. Accordingly, the drawings are to be regarded as illustrative in nature, and not as restrictive.

BRIEF DESCRIPTION OF THE DRAWINGS

Reference is made to the attached drawings, wherein elements having the same reference number designation represent like elements throughout.

Fig. 1 is a block diagram of an exemplary system in which an embodiment of the present invention may be employed.

Fig. 2 is a detailed diagram illustrating an exemplary implementation of the network switch of Fig. 1.

Fig. 3 is a flow diagram illustrating processing performed by the network switch of Fig. 1 according to an exemplary implementation of the present invention.

Fig. 4 is a block diagram illustrating the external memories of Fig.1 according to an exemplary implementation of the present invention.

Fig. 5 is a block diagram illustrating an exemplary sequence of selection signals from the scheduler and the bus activity on the external memory buses of Fig. 2.

BEST MODE FOR CARRYING OUT THE INVENTION

The present invention will be described with the example of a switch in a packet switched network, such as an Ethernet network. It will become apparent, however, that the present invention is also applicable to other packet switched systems, as described in detail below, as well as to other types of systems in general.

Fig. 1 is a block diagram of an exemplary system in which an embodiment of the present invention may be advantageously employed. The exemplary system 100 includes

a network switch 110 and memories 150 and 160. The system 100 may also include a packet switched network, such as an Ethernet network. The network may include a number of network stations (not shown) having different configurations. According to an exemplary implementation, the network may include twenty-four 100 megabit per second (Mb/s) stations that send and receive data packets at a rate up to 100 Mb/s and two 1000 Mb/s, (i.e., 1 gigabit per second, (Gb/s)) stations that send and receive data packets at a rate up to 1 Gb/s. Other network configurations may be used in alternative implementations of the present invention.

The switch 110 forwards data packets received from the network stations to the appropriate destinations based upon Ethernet protocol. The switch 110 may include media access control (MAC) units 120 and 130 and an external memory interface 140. The MAC units 120 and 130 may include MAC modules for each port supported by the switch. Each MAC module may include a MAC receive portion, a receive first-in first-out (FIFO) buffer, a transmit FIFO buffer and a MAC transmit portion. Data packets from the network stations are received by a corresponding MAC module and stored in the corresponding receive FIFO.

According to an exemplary implementation, MAC units 120 and 130 each include 12 MAC modules that support communications with twelve 100 Mb/s network stations and one MAC module that supports communication with one 1 Gb/s network station. In alternative implementations, the MAC units 120 and 130 may be combined into a single MAC unit or into other numbers of MAC units.

The external memory interface 140 enables external storage of data packets in external memories 150 and 160 via buses 170 and 180, respectively. In an exemplary implementation of the present invention, the external memories 150 and 160 may be synchronous static random access memory (SSRAM) devices. In alternative implementations, the external memories 150 and 160 may be other types of memory devices. As described previously, switch 110 controls the communication of data packets between network stations. Accordingly, the switch 110 includes various logic devices, such as switching subsystems, decision making logic and address tables, for receiving and forwarding the data packets to their respective destinations. Details of these logic devices are well known and are not shown or described in order not to unduly obscure the thrust of the present invention. The operation and structure of such devices, however, would be obvious to one of ordinary skill in this art.

Fig. 2 is a detailed block diagram of the network switch 110 of Fig.1 according to an exemplary implementation of the present invention. MAC unit 120 includes MAC modules MACP1-MACP12 corresponding to twelve 100 Mb/s ports on the switch 110 and MACG1 corresponding to a 1 Gb/s port on the switch 110. MAC unit 130 similarly includes twelve MAC modules MACP13-MACP24 corresponding to 100 Mb/s ports and MAC module MPG2 corresponding to a 1 Gb/s port.

External memory interface 140 may include multiplexers 210 and 220, scheduler 230 and switching logic 240. Multiplexer 210 receives data inputs from MAC modules MACP1-MACP12 and MACG1 and multiplexer 220 receives data inputs from MACP13-MACP24 and MACG2. The multiplexers 210 and 220 selectively output the data frame information from the MAC modules to switching logic 240 in accordance with signals from scheduler 230, as described in more detail below.

Scheduler 230 transmits selection signals to multiplexers 210 and 220 for selectively outputting data frame information from the MAC units 120 and 130. The multiplexers 210 and 220 receive the selection signals and then output the corresponding data frame information to switching logic 240. Switching logic 240 transfers the received data frame information to memories 150 and 160 and ensures that data from the multiplexers 210 and 220 does not get transferred to the same memory simultaneously, thereby avoiding bus contention problems. In alternative implementations, the functions performed by switching logic 240 may be performed by scheduler 230. That is, the scheduling and switching functions may be performed by a single device located in external memory interface 140.

Fig. 3 illustrates exemplary processing for storing data packets in memories 150 and 160, according to an exemplary implementation of the present invention. Processing begins upon start-up of switch 110. Assume that each of the network stations transmits data packets to the switch 110 (step 310). The MAC units 120 and 130 receive the data packets and the respective MAC modules store the data packets in their receive FIFO buffer (step 320).

The scheduler 230 controls the transfer of data from the MAC receive FIFOs to the external memories 150 and 160. In an exemplary embodiment of the present invention, scheduler 230 may allocate a fixed amount of bandwidth to each port. For example, the scheduler 230 may allocate a time "slot" to each port supported by the switch 110. The fixed time slots together form an arbitration cycle. Each time slot in the

arbitration cycle may be equivalent to one clock cycle in duration (a "1-clock slot") and each 1-clock slot may be allocated to a single port based on the predetermined priority.

In an exemplary implementation of the present invention, each MAC module transfers 64-bits (8 bytes) of data frame information to switching logic 240 during its 1-clock slot. The gigabit ports may have ten times as many slots as the 100 Mb/s ports since the Gb/s ports receive data packets at ten times the data rate of the 100 Mb/s ports. Other slots may also be reserved for other devices accessing the external memories 150 and 160 based on the particular network requirements.

In any event, the scheduler 230 simultaneously transmits selection or enable signals to multiplexers 210 and 220 to permit the multiplexers to output data from one of the corresponding MAC modules to switching logic 240, based on the predefined arbitration cycle (step 330). The multiplexers 210 and 220 receive the selection signals and transfer the data frame information from the corresponding MAC module to switching logic 240 (step 340). In alternative implementations, the scheduler 230 may receive signals from the MAC modules requesting access to the external memories 150 and 160 and grant priority based on the received request signals.

The switching logic 240 may simultaneously receive data from both multiplexers 210 and 220. The switching logic 240 may then simultaneously transfer the data frame information to memories 150 and 160 via data buses 170 and 180, respectively (step 350). According to an exemplary embodiment, each transfer is an individual transfer with an independent address associated with each transfer.

Fig. 4 illustrates memories 150 and 160 according to an exemplary embodiment of the present invention. Memory 150 may store odd-addressed words and memory 160 may store even-addressed words. That is, memory 150 may be configured with only odd addressed words, e.g., addresses 01, 03, 05, ... 2N+1, where N is an integer, and memory 160 may be configured with only even addressed words, e.g., addresses 00, 02, 04, ... 2N. According to the exemplary embodiment, the width of the data words in memories 150 and 160 is 8 bytes. In alternative implementations, other data widths may be employed. Switching logic 240, therefore, generates odd address information when writing data to memory 150 and even address information when writing the data frame information to memory 160. It should also be understood that the switching logic 240 transfers the data to the external memories 150 and 160 in a single clock cycle.

According to an exemplary embodiment, switching logic 240 continues to simultaneously write the data frame information to memories 150 and 160 in an alternating fashion (step 360). That is, the switching logic 240 writes data frame information received via one of the multiplexers to an odd addressed word in memory 150 while simultaneously writing data received from the other multiplexer to an even addressed word in memory 160. In this manner, 16-bytes of data are simultaneously written to external memories 150 and 160 in a single clock cycle and stored as two eight byte words. Alternating the bus privilege in this manner enables both external memory buses 170 and 180 to remain busy and maximizes the data throughput of network switch 110.

Fig. 5 illustrates the sequence of bus activity on memory bus 170 (i.e., the odd-address memory bus) and memory bus 180 (i.e., the even-address memory bus) according to an exemplary embodiment of the present invention. The sequence of selection or enable signals from scheduler 230 to multiplexers 210 and 220 is illustrated in columns A and B, respectively. As shown in column A, scheduler 230 outputs selection signals corresponding to the MAC ports in MAC unit 120, i.e., MP1 through MP12, and the 1 Gb/s MAC port, i.e., MG1, and repeats the cycle. As discussed previously, the 1 Gb/s ports may include 10 times as many slots as the 100 Mb/s ports and, therefore, the selection signals corresponding to the Gb/s ports may represent 10 slots. Alternatively, the sequence of selection signals may be modified to provide the gigabit port with an adequate number of slots in which to make its transfers. Scheduler 230 also outputs selection signals corresponding to the MAC ports in MAC unit 130, i.e., MP13 through MP24 and the 1 Gb/s port, i.e., MG2, in a similar manner.

Columns C and D in Fig. 5 represent the sequence of bus activity on memory buses 170 and 180, respectively, based on the sequence of enable signals in columns A and B. As described previously, the switching logic 240 simultaneously writes data frame information from multiplexers 210 and 220 to memories 150 and 160. For example, at the first time slot illustrated in Fig. 5, the switching logic 240 transfers 8 bytes of data frame information from MAC port 1 (MP1) to an even addressed word (MP1_EVEN) in memory 160 via memory bus 180, as illustrated by the first entry in column D. Also during the first time slot, the switching logic 240 transfers 8 bytes of data frame information from MAC port 13 (MP13) to an odd addressed word (MP13_ODD) in memory 150 via memory bus 170, as illustrated by the first entry in

column C. The switching logic 240 may then alternate the storage of data frame information received from multiplexers 210 and 220. That is, the switching logic 240 may transfer the next 8 bytes of data frame information received from multiplexer 210 to memory 150, as indicated by the second entry MP2_ODD in column C. The switching logic 240 may also transfer the next 8 bytes of data frame information received from multiplexer 220 to memory 160, as indicated by the second entry MP14_EVEN in column D.

The switching logic 240 continues this process of alternating the storage of data frame information from multiplexers 210 and 220 to memories 150 and 160. In this manner, the external memory interface 140 outputs 16 bytes at a time for storage in external memories 150 and 160. The external memory interface 140 may then retrieve the data frame information stored in memories 150 and 160 in a similar manner. That is, the external memory interface 140 may retrieve 16 bytes of data frame information during a single clock cycle via buses 170 and 180.

Described has been an apparatus and method for accessing external memories from a network switch. One advantage of the invention is that the width of the external memory buses 170 and 180 and the data width of the words in the external memories 150 and 160 is reduced to 8 bytes. This results in less wasted bandwidth when performing partial word transfers or when performing memory management involving buffer headers and enables the network switch 110 to meet the overall data throughput required in typical high speed networks.

For example, in typical systems, the external memory bandwidth needs to be large enough to accommodate the maximum transient network traffic. For a "24 + 2" switch (i.e., twenty-four 100 Mb/s ports and two 1 Gb/s ports), for example, the maximum incoming and outgoing bit rate on the network switch is ((24 X 100) Mb/s + (2 X 1000) Mb/s)) X 2, or 8.8 Gb/s. That means that the bus width times the bus frequency must be greater than 8.8 Gb/s. The present invention has been found to advantageously achieve data throughput in excess of the required 8.8 Gb/s rate when using a 100 MHz external bus frequency. Therefore, the present invention advantageously supports high data throughput requirements and increases bus efficiency.

Only the preferred embodiments of the invention and a few examples of its versatility are shown and described in the present disclosure. It is to be understood that

the invention is capable of use in various other combinations and environments and is capable of modifications within the scope of the inventive concept as expressed herein.

For example, the present invention has been described with the example of a multiport network switch storing and retrieving data frame information to and from external memories. The present invention is also applicable to other situations involving access to external memories where bus efficiency is of importance.

WHAT IS CLAIMED IS:

1. A network switch configured to control communication of data frames between stations, comprising:

a plurality of receive devices corresponding to ports on the network switch, the receive devices configured to receive data frames from the stations; and

an external memory interface configured to receive data from the plurality of receive devices, transfer a portion of the data received from a first one of the receive devices to a first memory, and transfer a portion of the data received from a second one of the receive devices to a second memory.

2. The network switch of claim 1, wherein the external memory interface includes:

a scheduler coupled to the receive devices and configured to enable the received data frames to be output to the first and second memories, the scheduler simultaneously outputting first and second selection signals for outputting data from the first receive device and the second receive device, respectively.

3. The network switch of claim 2, wherein the external memory interface is further configured to simultaneously transfer 8 bytes of data from the first receive device to the first memory and 8 bytes of data from the second receive device to the second memory.

4. The network switch of claim 1, wherein the external memory interface is further configured to simultaneously transfer the portions of the data from the first and second receive devices to the first and second memories.

5. The network switch of claim 1, wherein the external memory interface includes a first external memory bus and a second external memory bus, and the external memory interface is configured to simultaneously transfer data received from a first one of a first group of the receive devices via the first external memory bus and a second one of a second group of the receive devices via the second external memory bus.

6. The network switch of claim 5, wherein the external memory interface is further configured to alternately transfer data received from the first group of receive devices to the first and second memories and to alternately transfer data received from the second group of receive devices to the first and second memories.

7. The network switch of claim 5, wherein the first and second external memory buses are each 8-bytes wide and operate at a frequency of 100 MHz.

8. The network switch of claim 1, wherein the external memory interface includes a first external memory bus to transfer data to the first memory and a second external memory bus to transfer data to the second memory, the external memory interface being further configured to generate odd address information when transferring data via the first external memory bus and even address information when transferring data via the second external memory bus.

9. The network switch of claim 1, wherein the external memory interface is further configured to simultaneously retrieve data from the first and second memories.

10. In a network switch that controls communication of data frames between stations, a method of storing data frame information, comprising:

receiving a plurality of data frames;

temporarily storing the received data frames; and

simultaneously transferring data frame information to at least a first memory and a second memory.

11. The method of claim 10, wherein the data frames are temporarily stored in a plurality of receive devices, further comprising:

simultaneously transmitting selection signals to first and second receive devices for selectively outputting data stored in the first and second receive devices.

12. The method of claim 10, wherein the simultaneous data transferring includes:

transferring 8 bytes of data from a first receive device to the first memory and 8 bytes of data from a second receive device to the second memory.

13. The method of claim 10, wherein the simultaneously transferring includes:

sending a portion of a first data frame via a first external memory bus and sending a portion of a second data frame via a second external memory bus.

14. The method of claim 10, wherein the data frames are temporarily stored in a plurality of receive devices, further comprising:

alternately transferring data frame information from a first group of the receive devices to the first and second memories; and

alternately transferring data frame information from a second group of the receive devices to the first and second memories.

15. The method of claim 10, further comprising:

simultaneously retrieving data frame information from the first and second memories.

16. A data communication system for controlling the communication of data frames between stations, comprising:

a plurality of receive devices configured to receive data frames from the stations;

a scheduler coupled to the plurality of receive devices and configured to generate selection signals to selectively output data frame information from the receive devices; and

a switching device configured to receive the data frame information and to simultaneously transfer data frame information from a first one of the data frames via a first external memory bus and data frame information from a second one of the data frames via a second external memory bus.

17. The system of claim 16, further comprising:

first and second multiplexers coupled to first and second groups of the receive devices, respectively, each of the first and second multiplexers being configured to receive the selection signals from the scheduler and to output a portion of a data frame.

18. The system of claim 17, wherein the switching device is further configured to alternately transfer data received from the first multiplexer to the first and second external

memory buses and to alternately transfer data received from the second multiplexer to the first and second external memory buses.

19. The system of claim 16, further comprising:

a first memory coupled to receive data frame information from the first external memory bus and configured to store data words having odd addresses; and

a second memory coupled to receive data frame information from the second external memory bus and configured to store data words having even addresses.

20. The system of claim 19, wherein the switching logic is configured to generate data address information having odd addresses for data transferred to the first memory and generate data address information having even addresses for data transferred to the second memory.

ABSTRACT OF THE DISCLOSURE

A network switch that controls the communication of data frames between stations includes receive devices that correspond to ports on the network switch. The receive devices receive and store data frame information from the network stations. The network switch also includes an external memory interface that receives the data frame information from the receive devices and transfers the data frame information to multiple external memory devices.

100

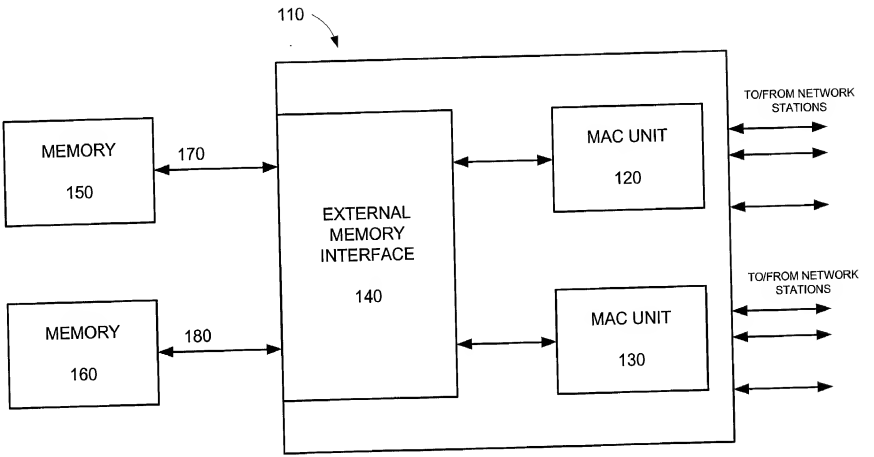

FIG.1

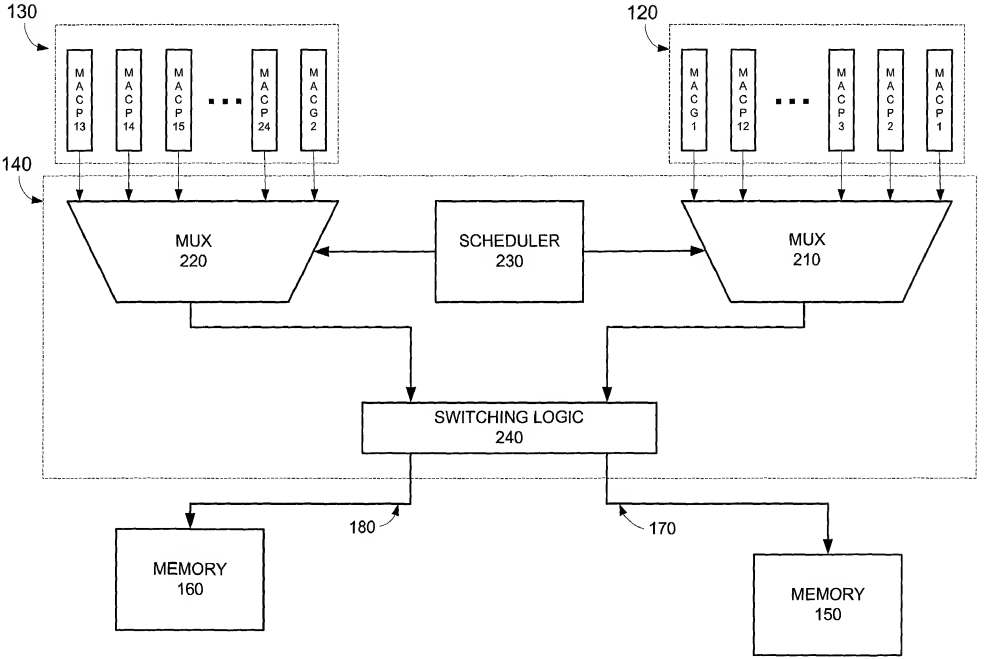
130
MACP13
MACP14
MACP15
MACP24
MACG2
120
MACG1
MACP12
MACP3
MACP2
MACP1
140
MUX
220
SCHEDULER
230
MUX
210
SWITCHING LOGIC
240
180
170
MEMORY
160
MEMORY
150

FIG. 2

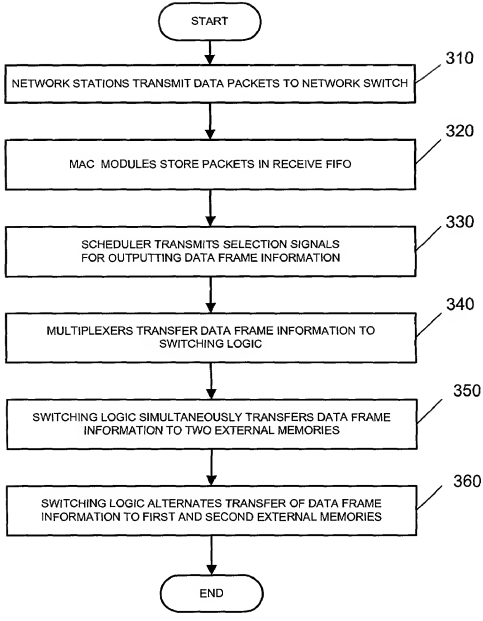
START
NETWORK STATIONS TRANSMIT DATA PACKETS TO NETWORK SWITCH
310
MAC MODULES STORE PACKETS IN RECEIVE FIFO
320
SCHEDULER TRANSMITS SELECTION SIGNALS FOR OUTPUTTING DATA FRAME INFORMATION
330
MULTIPLEXERS TRANSFER DATA FRAME INFORMATION TO SWITCHING LOGIC
340
SWITCHING LOGIC SIMULTANEOUSLY TRANSFERS DATA FRAME INFORMATION TO TWO EXTERNAL MEMORIES
350
SWITCHING LOGIC ALTERNATES TRANSFER OF DATA FRAME INFORMATION TO FIRST AND SECOND EXTERNAL MEMORIES
360
END

FIG. 3

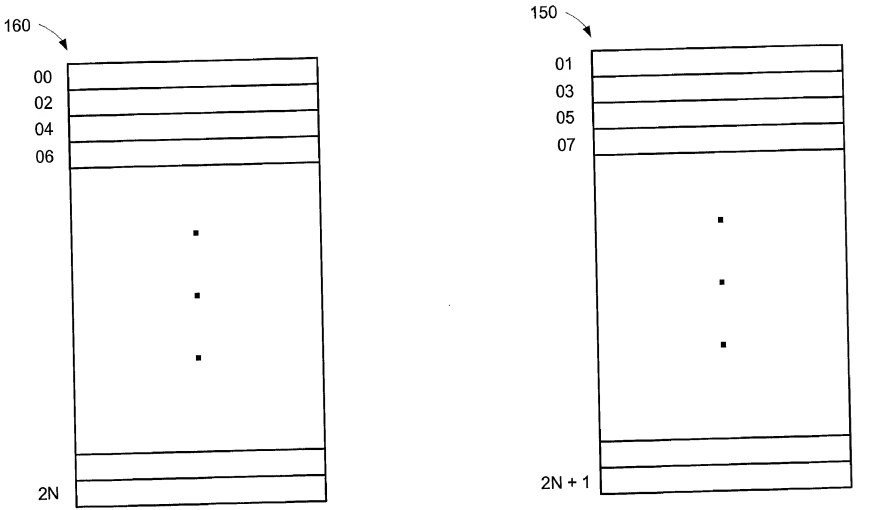

FIG. 4

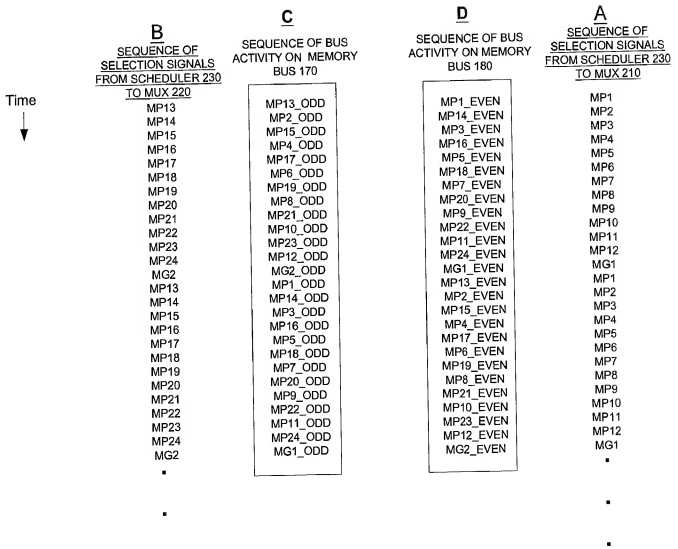
Time
B
SEQUENCE OF SELECTION SIGNALS FROM SCHEDULER 230 TO MUX 220
MP13
MP14
MP15
MP16
MP17
MP18
MP19
MP20
MP21
MP22
MP23
MP24
MG2
MP13
MP14
MP15
MP16
MP17
MP18
MP19
MP20
MP21
MP22
MP23
MP24
MG2
C
SEQUENCE OF BUS ACTIVITY ON MEMORY BUS 170
MP13_ODD
MP2_ODD
MP15_ODD
MP4_ODD
MP17_ODD
MP6_ODD
MP19_ODD
MP8_ODD
MP21_ODD
MP10_ODD
MP23_ODD
MP12_ODD
MG2_ODD
MP1_ODD
MP14_ODD
MP3_ODD
MP16_ODD
MP5_ODD
MP18_ODD
MP7_ODD
MP20_ODD
MP9_ODD
MP22_ODD
MP11_ODD
MP24_ODD
MG1_ODD
D
SEQUENCE OF BUS ACTIVITY ON MEMORY BUS 180
MP1_EVEN
MP14_EVEN
MP3_EVEN
MP16_EVEN
MP5_EVEN
MP18_EVEN
MP7_EVEN
MP20_EVEN
MP9_EVEN
MP22_EVEN
MP11_EVEN
MP24_EVEN
MG1_EVEN
MP13_EVEN
MP2_EVEN
MP15_EVEN
MP4_EVEN
MP17_EVEN
MP6_EVEN
MP19_EVEN
MP8_EVEN
MP21_EVEN
MP10_EVEN
MP23_EVEN
MP12_EVEN
MG2_EVEN
A
SEQUENCE OF SELECTION SIGNALS FROM SCHEDULER 230 TO MUX 210
MP1
MP2
MP3
MP4
MP5
MP6
MP7
MP8
MP9
MP10
MP11
MP12
MG1
MP1
MP2
MP3
MP4
MP5
MP6
MP7
MP8
MP9
MP10
MP11
MP12
MG1

FIG. 5

Docket No. F0255

DECLARATION AND POWER OF ATTORNEY

As a below named inventor, I hereby declare that: my residence, post office address and citizenship are as stated below next to my name; I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled: METHOD AND APPARATUS FOR ACCESSING EXTERNAL MEMORIES, the specification of which is attached hereto.

I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claims, as amended by any amendment referred to above. I acknowledge the duty to disclose information which is material to the examination of this application in accordance with Title 37, Code of Federal Regulations, § 1.56.

I hereby claim foreign priority benefits under 35 U.S.C. § 119(a)-(d) or § 365(b) of any foreign application(s) for patent or inventor's certificate or § 365(a) of any PCT international application(s), designating at least one country other than the United States, listed below and have also identified below any foreign application(s) for patent or inventor's certificate, or any PCT international application(s) having a filing date before that of the application(s) of which priority is claimed:

Country	Application Number	Date of Filing	Priority Claimed Under 35 U.S.C. 119
			☐ YES ☐ NO
			☐ YES ☐ NO

I hereby claim the benefit under 35 U.S.C. § 119(e) of any United States provisional application(s) listed below:

Application Number	Date of Filing

I hereby claim the benefit under 35 U.S.C. § 120 of any United States application(s) or § 365(c) of any PCT international application(s) designating the United States, listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States or PCT international application(s) in the manner provided by the first paragraph of 35 U.S.C. § 112, I acknowledge the duty to disclose information which is material to patentability as defined in 37 CFR § 1.56 which became available between the filing date of the prior application(s) and the national or PCT international filing date of this application:

U.S. Applications		Status (Check One)		
U.S. Application Number	U.S. Filing Date	Patented	Pending	Abandoned

PCT Applications Designating the U.S.					
PCT Application No.	PCT Filing Date	U.S. Serial Number Assigned (if any)			

I hereby appoint the following attorney and/or agent(s) with full power of substitution and revocation, to prosecute this application and transact all business in the Patent and Trademark Office connected therewith: Paul A. Harrity, Reg. No. 39,574; Glenn Snyder, Reg. No. 41,428; John E. Harrity, Reg. No. 43,367; and Tony M. Cole, Reg. No. 43,417; all of

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I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under section 1001 of Title 18 of the United States Code, and that such willful false statements may jeopardize the validity of the application or any patent issuing thereon.

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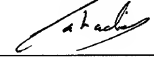
Full Name of Second Inventor Bahadir Erimli	Inventor's Signature 	Date Aug. 22, 2003
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